AF/JFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	**Mehran MOKHTARI**	Examiner:	Peguy JEAN PIERRE
Serial No.:	**10/772,113**	Art Unit:	2819
Filed:	February 3, 2004	Our Ref:	B-5100 620982-2
For:	"REPROGRAMMABLE DISTRIBUTED REFERENCE LADDER FOR ANALOG-TO-DIGITAL CONVERTERS"	Date:	September 30, 2005
		Re:	***Appeal to the Board of Appeals***

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection, dated July 1, 2005, for the above identified patent application. Enclosed please find a check in the amount of $500.00 for the fee set forth in 37 C.F.R. 1.17(c) for submitting this Brief. The Appellant submits that this Appeal Brief is being timely filed, since the notice of Appeal was filed concurrently.

REAL PARTY IN INTEREST

The present application has been assigned to HRL Laboratories, LLC of Malibu, CA.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to the present application.

STATUS OF CLAIMS

Claims 1 - 14 are the subject of this Appeal and are reproduced in the accompanying appendix.

STATUS OF AMENDMENTS

No Amendment After Final Rejection has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention described and claimed in the present application relates generally to analog-to-digital converters (ADCs), and more particularly to a novel distributed resistor ladder structure for use with flash ADCs (p. 1, ll. 11-13). As with most ADCs known in the art, the ADC of the present invention comprises a plurality of comparators, each comparator for comparing the voltage of the input signal to the ADC with the voltage of a reference signal (p. 8, ll. 13-16). In the ADCs known in the art, a single reference signal is input into a resistive ladder network and the reference signal for each comparator is tapped off at each resistor in the network (p. 1, l. 16 – p. 2, l. 2). An important novel feature of the ADCs of the present invention is that each comparator receives a reference signal supplied by a respective dedicated reference voltage generator (p. 8, ll. 16-19). Each such reference voltage generator is supplied with a supply voltage and may optionally be further supplied with a calibration voltage (p. 8, l. 19 – p. 9 l. 1). Thus, the ADC design of the present invention confers the important advantage of allowing calibration of the output reference voltage by adjusting an input voltage rather than a resistance, as previously accomplished in the art, and thus may be calibrated and even adjusted to different sampling setpoints after production (p. 11, ll. 10-18).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Issue 1: Whether Claims 1 – 3 and 9 - 11 are patentable under 35 U.S.C. 103(a) over U.S. Pat. No. 5,831,567 to Seki et al. (hereinafter "Seki") in view of U.S. Pat. No. 6,281,828 to Kimura et al. (hereinafter "Kimura").

GROUPING OF CLAIMS

For each ground of rejection which Appellant contests herein and which applies to more than one claim, such additional claims, to the extent separately identified and argued below, do not stand or fall together.

ARGUMENT

Issue 1: Whether Claims 1 – 3 and 9 - 11 are patentable under 35 U.S.C. 103(a) over U.S. Pat. No. 5,831,567 to Seki et al. (hereinafter "Seki") in view of U.S. Pat. No. 6,281,828 to Kimura et al. (hereinafter "Kimura").

In section 2 of the Office Action of July 1, 2005, the Examiner rejects claims 1-3 and 9-11 as being unpatentable over Seki in view of Kimura. In particular, the Examiner finds that Kimura discloses all claimed limitations except for a plurality of reference circuits, each coupled to a respective one of a plurality of comparators, and that Seki discloses an ADC that comprises a plurality of comparators and a plurality of reference circuits where each comparator compares on input electrical signal with a respective pre-selected reference voltage to eliminate DC offset which is contained in the analog signal. The Examiner thus opines that it would have been obvious to the skilled person to modify the reference voltage generator of Kimura by coupling individual reference circuits having pre-selected reference voltages to each comparator as taught by Seki "to improve performance and accuracy of the converter."

In the reply filed on May 5, 2005, Appellant explained why the Examiner's conclusion is not supported by the plain language of the two references, and also showed that if the skilled

person attempted to combine these two references, the result would not in fact be anticipatory of the present invention. In particular, Appellant explained that Kimura addresses the problem inherent in prior art ADCs of equivalent input offset due to device mismatch arising out of the manufacturing process. Kimura attempts to solve this problem by feeding the reference voltage to each comparator through a differential amplifier that is operated sequentially in two modes (normal and inverted) and the results of which are subtracted, to thereby eliminate any signal mismatch due to device mismatch among the various comparators. To support this interpretation Appellant noted that Kimura does not even mention DC offset in the input analog signal, much less discuss it as being a problem in the ADC that is disclosed, and also that more importantly, Kimura requires that the same reference voltage be used through all signal switching sections in order for the disclosed method of inverting and averaging the input analog signal and the reference signal to work. Kimura emphasizes this by disclosing an embodiment that provides multiple reference voltage signals that can be averaged to further reduce possible mismatch error (col. 8, ll. 3-53). Thus, applying the different reference voltage levels of Seki to Kimura would in fact produce a non-functioning device, and a skilled person attempting to practice the invention of Kimura would find absolutely no motivation to think of applying different reference voltage levels to the different comparator lines.

Appellant further noted that Seki does not actually disclose an ADC of the type disclosed by Kimura or of the type claimed by Appellant. Rather, the device of Seki is aimed at simply providing a binary digital signal R that tracks the frequency of an input analog signal regardless of the DC offset of the input analog signal. It is for this reason that Seki provides the different reference voltage levels V_{refi}, as the Examiner acknowledged in the first Office Action. As clear from, *inter alia*, Figs. 15D and 17G, the output signal R of the device of Seki merely tracks the change in phase of the AC component of the amplified input analog signal A. Thus, a skilled person looking to develop or improve an ADC as disclosed by Kimura would not consider applying Seki, as Seki does not in fact disclose a device that provides a digital signal indicative of the voltage or magnitude of an input analog signal (i.e. an ADC as typically understood by those skilled in the art and as disclosed by Kimura) but rather indicative of the frequency of the input signal.

In the final Action, the Examiner responds to Appellant's arguments by agreeing that Kimura indeed does not mention DC offset in the input analog signal nor discuss it as being a problem in the ADC, and further acknowledging that Kimura uses the same reference voltage in all switching sections. However, the Examiner retorts that "there is no limitation of a 'DC offset in the input analog signal. Has such limitation been recited in the rejected claims, the reference (Kimura) meets the language because it discloses a comparator coupled to a plurality of encoders." Appellant has difficulty comprehending what this means. Erstwhile, Appellant's main argument is that applying the teachings of Seki to Kimura would in fact produce a nonfunctional device. The existence of a DC offset in the input analog signal is a problem inherent in prior art devices, and has no bearing upon the inventive features of Appellant's invention, and it is entirely unclear why the Examiner seizes upon this statement of Appellant and completely ignores the fundamental flaw that these two references cannot in fact be combined into one device as alleged by the Examiner.

The Examiner also disagrees that the Seki reference generates a digital signal indicative of the frequency of the input signal, but offers nothing more in support of this beyond that "[t]he field of the invention clearly states the generation of the digital signal based on the analog signal." Appellant is at a complete loss as to how this proves the Examiner's assertion, especially in light of the clear language of Seki: "[t]he present invention relates ...more particularly, to a method and signal processing apparatus for generating a digital signal based on an alternating current (AC) signal component contained in an analog signal." Seki clearly teaches that the digital signal is generated in response to a plurality of *pulse signals* that are themselves generated in response to *level transitions* in the input signal. The Examiner is in essence ignoring Appellant's argument, namely that Seki does not use the reference voltages in a manner similar to Kimura, and once again chooses to focus on irrelevant statements and misinterpret them.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP §2142. The Examiner has set forth not the slightest hint of

such motivation, real or otherwise, in either of the cited references nor has he invoked the general knowledge of those skilled in the art. To merely state the benefit conferred by the invention is not setting forth the required showing of motivation but rather merely applying the benefit of hindsight to its fullest in combining disjointed references with the benefit of the invention itself as an explicit roadmap.

"Second, there must be a reasonable expectation of success... The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." MPEP §2142. The Examiner has offered not one single detail as to how exactly the skilled person would go about modifying the reference voltage generator of Kimura by coupling individual reference circuits having pre-selected reference voltages to each comparator as taught by Seki. As Appellant has set forth in detail, this is not in fact practically feasible, and the Examiner's dismissive assertions to the contrary fall far short of the burden imposed by the Rules and the MPEP.

In light of the above, Appellant submits that the cited art is not a proper combination to support a rejection in the present case, that even if combined the result would not read upon the present claims and would not even provide a functional device, and that claims 1 and 9 are therefore novel and nonobvious over the art of record, and thus respectfully requests that the Examiner be overturned on Appeal and these claims be passed to issue.

Claims 2-8 depend from claim 1 and claims 10-14 depend from claim 9. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion, Appellant submits that claims 2-8 and 10-14 are also allowable.

CONCLUSION

For the extensive reasons advanced above, Appellant respectfully contends that each claim is patentable. Therefore, reversal of all rejections and objections and re-opening of the prosecution is respectfully solicited.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

September 30, 2005
(Date of Transmission)

Alma Smalling
(Name of Person Transmitting)

Alma Smalling
(Signature)

9/30/05
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Attachments

Claims

1. (original) An analog to digital converter, comprising:

a plurality of comparators, each comparator for comparing an input electrical signal with a respective, pre-selected reference electrical signal;

an encoder coupled to the comparators to receive a detection signal from each comparator indicative of the input signal; and

a plurality of reference circuits, each reference circuit coupled to a respective one of the plurality of comparators to supply the respective reference electrical signal to the respective comparator.

2. (previously presented) The analog to digital converter of claim 1, wherein each comparator comprises:

a comparator for comparing a voltage of the input electrical signal with a voltage of the respective reference electrical signal, the respective reference electrical signal having a pre-selected voltage.

3. (previously presented) The analog to digital converter of claim 2, wherein the encoder comprises:

an encoder to receive the detection signal from each comparator indicative of an input signal voltage.

4. (original) The analog to digital converter of claim 3, wherein each reference circuit comprises:

an output transistor to provide the reference electrical signal;

a current source coupled between an emitter of the output transistor and ground;

a reference resistor coupled to a base of the output transistor to set an operation current of the output transistor;

a control transistor coupled to the reference resistor in parallel with the output transistor to allow current flow through the reference resistor; and

a current mirror coupled in parallel with the reference resistor and control transistor to control the current flowing through the reference resistor.

5. (original) The analog to digital converter of claim 4, wherein the current mirror comprises:

a resistor coupled in series with a transistor.

6. (original) The analog to digital converter of claim 3, wherein each reference circuit comprises:

an emitter follower circuit.

7. (original) The analog to digital converter of claim 4, wherein the current mirror comprises:

a trans-admittance amplifier coupled in series with a transistor.

8. (original) The analog to digital converter of claim 3, wherein each reference circuit comprises:

an output transistor to provide the reference electrical signal;

a current source coupled between an emitter of the output transistor and ground;

a reference resistor coupled to a base of the output transistor to set an operation current of the output transistor;

a control transistor coupled to the reference resistor in parallel with the output transistor to allow current flow through the reference resistor; and

a trans-admittance amplifier coupled to the base of the control transistor to control the current flowing through the reference resistor.

9. (previously presented) A method for digitizing an analog signal, comprising:

generating a plurality of predetermined reference

electrical signals;

supplying each reference electrical signal to a respective one of a plurality of comparators;

supplying an input electrical signal to each one of the comparators to compare the input electrical signal with the respective reference electrical signal and to provide a detection signal indicative of the input electrical signal; and

providing each detection signal from each comparator to an encoder arranged to output a signal indicative of a magnitude of the input electrical signal.

10. (original) The method of claim 9, wherein generating the plurality of predetermined reference electrical signals comprises:

generating each reference electrical signal at a preselected voltage.

11. (original) The method of claim 10, wherein supplying the input electrical signal to each one of the comparators comprises:

supplying the input electrical signal to each one of the comparators to provide a detection signal indicative of an input signal voltage.

12. (original) The method of claim 11, wherein generating each predetermined reference electrical signal comprises:

applying a supply voltage to each of a plurality of emitter follower circuits to generate each predetermined reference electrical signal at the respective preselected voltage.

13. (previously presented) The method of claim 12, wherein generating each predetermined reference electrical signal comprises:

applying the supply voltage to each of a plurality of reference circuits, each reference circuit comprising an output transistor to provide the reference electrical signal, a current source coupled between an emitter of the output transistor and ground, a reference resistor coupled to a base of the output transistor to set an operation current of the output transistor, a control transistor coupled to the reference resistor in parallel with the output transistor to allow current flow through the reference resistor, and a current mirror coupled in parallel with the reference resistor and control transistor to control the current through the reference resistor, the current mirror comprising a trans-admittance amplifier coupled in series with a transistor; and

applying a preselected control current to the trans-admittance amplifier to control the current flowing through the reference resistor to cause the output transistor to provide the reference electrical signal at the respective preselected voltage.

14. (previously presented) The method of claim 12, wherein generating each predetermined reference electrical signal comprises:

applying the supply voltage to each of a plurality of reference circuits, each reference circuit comprising an output transistor to provide the reference electrical signal, a current source coupled between an emitter of the output transistor and ground, a reference resistor coupled to a base of the output transistor to set an operation current of the output transistor, a control transistor coupled to the reference resistor in parallel with the output transistor to allow current flow through the reference resistor, and a trans-admittance amplifier coupled to the base of the control transistor to control the current through the reference resistor; and

applying a preselected control current to the trans-admittance amplifier to control the current flowing through the reference resistor to cause the output transistor to provide the reference electrical signal at the respective preselected voltage.

There is no evidence submitted with the present Brief on Appeal.

There are no other appeals or interferences related to the present application.